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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/824,932
Filing Date: April 15, 2004
Appellant(s): RUAT ET AL.

MICHAEL W. TAYLOR
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/4/2008 appealing from the Office action mailed 5/2/2008

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 4907225	Gulick et al.	03-1990
US 5072374	Sexton et al.	12-1991
US 6091737	Hong et al.	07-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 6, 8 – 9, 10 – 15, 17, 18 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick et al. (US 4,907,225) in view of Applicant Admitted Prior Art (hereafter referred to as AAPA) and further in view of Sexton et al. (US 5,072,374) and Hong et al. (US 6,091,737).

Regarding claim 1, Gulick discloses an asynchronous frame receiver (Abstract; column 2, lines 59 – 68; column 3, lines 15 – 17) comprising:

an input to receive asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters;

a break character detection unit to detect the break character (column 3, lines 15 – 17; Fig. 21, element 412 break checker; column 37, lines 30 - 33);

a standard character processing unit to detect the standard characters (column 35, lines 10 – 52; column 38, lines 21 – 34);

a first operating mode where only the standard character processing unit is to operate (column 37, lines 30 – 33; wherein the break character detection does not take place in the synchronous mode);

and a second operating mode where said break character detection unit to activate said standard character processing unit after the character break has been detected (column 35, lines 10 – 52; column 38, lines 21 – 34).

Gulick does not explicitly disclose an input for receiving asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters and that the break character detection unit comprises a first state machine, and the standard character processing unit comprises a second state machine.

In the same field of endeavor, however, AAPA discloses an input for receiving asynchronous frames comprising standard characters, and a header comprising a break character (Applicant's Prior Art Figure 1; wherein the header is the BRK + SYNC section of the frame).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by AAPA, in the system of Gulick

because this would allow the UART to conform to the specification of the LIN protocol, as disclosed by the AAPA (Specification, page 2, paragraph 5).

In the same field of endeavor, however, Sexton discloses a header comprising a break character with a data bit length greater than a data bit length of the standard characters (column 3, lines 27 – 31).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Sexton, in the system of Gulick because this would allow the UART to conform to the specification of the communication protocol, so that it could communicate properly with other devices.

In the same field of endeavor, however, Hong discloses the break character detection unit comprises a first state machine, and the standard character processing unit comprises a second state machine (Fig. 22, element 198, 202; column 38, lines 1 – 41; wherein the break character detection function is the performed by the part of the state machine 198 and the standard character processing function is performed by the different part of the state machine 202). Though Hong discloses elements 198 and 202 in a single state machine, one of ordinary skill in the art can easily separate the two elements into two separate state machines to allow the break characters to be detected first and then the standard characters. As per MPEP 2144.04 (section V, Item C), separating parts of prior art to obtain the same functionality is not considered patentable. Further, since the break character detection is not operable in the first

operating mode, one of ordinary skill in the art can easily not use the break character state machine and use only the standard character state machine.

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Hong, in the system of Gulick because this would allow the break characters to be detected first and then the standard characters.

Regarding claim 2, Gulick discloses a selection circuit for selecting a first operating mode in which said break character detection unit is deactivated, or a second operating mode in which said break character detection unit is active and controls said standard character processing unit (column 3, lines 15 – 29; column 37, lines 30 – 33; wherein since the break detection is performed in asynchronous mode, selection of asynchronous or synchronous mode is equivalents to activating or deactivating the break character detection unit).

Regarding claim 3, Gulick discloses break character detection unit detects a break character formed of bits having a same value (column 38, lines 21 – 24; wherein the same values is interpreted as the all ZEROS that are transmitted).

Regarding claim 4, Gulick discloses the asynchronous frames comprise a synchronization character, and wherein said break character detection unit detects the synchronization character (column 10, lines 30 – 37; column 19, line 42 – column 20, line 2; wherein the synchronization character is interpreted as the SFS signal and the

break character detection unit detecting the synchronization character is done by when the first 8 bits of the frame are located).

Regarding claim 5, Gulick discloses a self-synchronization circuit for synchronizing a local clock signal of the receiver with a reference clock signal in the synchronization character (column 41, line 65 – column 42, line 13; wherein synchronizing the local clock to the reference clock is interpreted as host request signal being synchronized with the local clock signal).

Regarding claim 6, Gulick discloses said self-synchronization circuit is activated by said break character detection unit (column 10, lines 30 – 37; column 19, line 42 – column 20, line 2; column 41, line 65 – column 42, line 13; wherein the activation of the self-synchronization circuit is interpreted as being done by the HREQ signal).

Regarding claim 8 , Gulick discloses selection circuit comprises a register for storing a mode bit (column 3, line 15 - 21)

Regarding claim 9 , Gulick discloses a substrate, and wherein said break character detection unit and said standard character processing unit are on said substrate so that the receiver comprises an integrated circuit (column 2, lines 41 – 58; wherein break character detection unit and the standard character processing unit on an integrated circuit is interpreted as the controller being on a single integrate circuit).

Claim 10 – 15, 17 are similarly analyzed as claims 1 – 6, 8 respectively.

Claims 18 - 23 are directed to method/steps of the same subject matter claimed in apparatus claims 1 - 6 respectively and therefore, are rejected as explained in the rejections of claims 1 - 6 above.

(10) Response to Argument

1. Argument: Appellant argued that:

   Since the first state machine is configured to detect the break character within the header, it ensures a complete detection of the frame header before activating the second state machine for detecting the standard characters (when in the second operating mode) (Appeal Brief 12/4/2008, page 9, 1st paragraph);

   and

   In sharp contrast, for the second operating mode of the first and second state machines in the claimed invention, the second state machine (i.e., break character detection unit) activates the first state machine (i.e., standard character processing unit) after the character break has been detected. This is not always possible with Hong et al. (Appeal Brief 12/4/2008, page 9, last paragraph).

Response: Firstly, examiner would like to point out that the Appellant has mixed up the definition of the 1^{st} and 2^{nd} state machines in the Appeal Brief on page 9, last paragraph, lines 7 - 9). Appellant has here called the 2^{nd} state machine, the break character detection unit, and the 1^{st} state machine the standard character detection unit. Previously, in the Appeal Brief, (page 3, 1^{st} 4 lines). Appellant has called the 1^{st}

state machine SM1 as the break character detection unit and the 2nd state machine SM2 as the standard character detection unit. However, from the context and from the specification (see [0009], [0010]) it is clear that in the Appellant's invention, the standard character detection unit is activated by the break character detection unit and therefore the Examiner has assumed this below.

Examiner respectfully disagrees with Appellant's argument. As stated in the Advisory Action (7/28/2008, page 2, Argument a) In Hong's Fig. 22, the break characters are clearly detected first in block 198 before the standard characters are detected in block 202. Also see column 38, lines 18 – 27, from which it is clear that only if the expected (i.e. correct) sync-byte is received does the flow pass to blocks 200 and 202. Therefore, Examiner contends that the standard character detection block 202 is executed only after the break character detection block 198 is executed.

2. Argument: Appellant argued that in his invention one advantage is that two operating modes are supported (Appeal Brief 12/4/2008, page 9, 2nd paragraph (indented one); page 10, 1st full paragraph).

Response: As stated in the Advisory Action (7/28/2008, page 2), Examiner maintains that this would be true in Hong's system as well. If the state machine was separated into 2 state machines, one of ordinary skill in the art can easily use only one or both as needed, thereby still having two modes.

3. Argument: Appellant argued that:

> The claims in the present invention recite that the asynchronous frames comprise standard characters, and a header comprises a break character BRK with a data bit length greater than a data bit length of the standard characters. The Examiner is using a three way rejection to provide this feature of the claimed invention (Appeal Brief 12/4/2008, page 10, 2nd full paragraph);
>
> and,
>
> The Appellants submit that is would not have been obvious to selectively combine the prior art references as suggested by the Examiner to produce this feature of the claimed invention. This is particularly so since the Sexton et al. patent fails to disclose that the controllers are operating as asynchronous frame receivers. Instead, the controllers in Sexton et al. communicate with each other via a common bus under the control of a master controller (Appeal Brief 12/4/2008, page 11, 1st full paragraph).

Response: Examiner respectfully disagrees. Firstly, as stated in the Advisory Action (7/28/2008, page 3), Sexton is being used to disclose the header comprising a break character with a data bit length greater than a data bit length of the standard characters. Therefore, Appellant's argument that Sexton fails to disclose that the controllers are operating as asynchronous frame receivers is not really relevant. Secondly, though Sexton may not explicitly state whether his system is synchronous or asynchronous, it is obvious to one of ordinary skill in the art that the system is

asynchronous (column 2, lines 3 – 31), since the slave PLCs have to monitor for a break character and because the length of the message is transmitted, implying variable length messages.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Adolf DSouza

Assistant Examiner

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